A New Model For Enhancement-Mode Power pHEMT

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***Abstract*—Optimum loading for a power enhancement-mode pseudomorphic high electron-mobility transistor (E-pHEMT) is determined by a systematic harmonic load–pull simulation. The simulation uses a modified Angelov–Parker model that can accurately predict dc, small-signal RF, and power performance of the devices. The optimum second harmonic loading for a 2-mm device is found to be open circuit and the optimum third harmonic is at the third quadrant, which is about $1\angle 210°$. The measured versus modeled results show very good agreement and, therefore, verify the model. The simulation predicts that as high as 80% power-added efficiency can be achieved for E-pHEMT under optimum source and load termination with harmonic tuning.**

I. Introduction

ENHANCEMENT-MODE pseudomorphic high electron-mobility transistors (E-pHEMTs) have been of great interest in wireless communication applications because they feature single supply operation while keeping the features of high power-added efficiency (PAE) and high power gain [1]. However, a good model formulation for E-pHEMTs is still lacking. Design of an E-pHEMT power amplifier is still based on experimental load–pull at each harmonic, which is very time consuming. Therefore, it is highly desirable to rely on simulation of load–pull.

To perform an accurate simulation of load–pull at each harmonic, it is essential to have a good model for the device. Many commercial models for MESFETs and pHEMTs are found not to be satisfactory because they lack accurate capacitance and dispersion models. The Angelov model [2] gives a very good description of dc characteristics and the Statz and Parker charge models [3] satisfy the charge conservation and describe very well the pinchoff of gate–source capacitance. The dispersion effects, including self-heating and the difference of RF $G_{\rm ds}$ and RF G_m from those at dc, have been accounted for in the Alpha model [4]. In this paper, we combined all the features of the models into an accurate and comprehensive model. In this new model, both formulations of the modified Angelov dc and Alpha owned model (AOM) charge model are used.

Harmonic load–pull simulation has been reported previously [5]. In this paper, a harmonic load element in series IV is created that allows separate harmonic tuning or optimization at each harmonic. Using the harmonic load makes the simulation very efficient.

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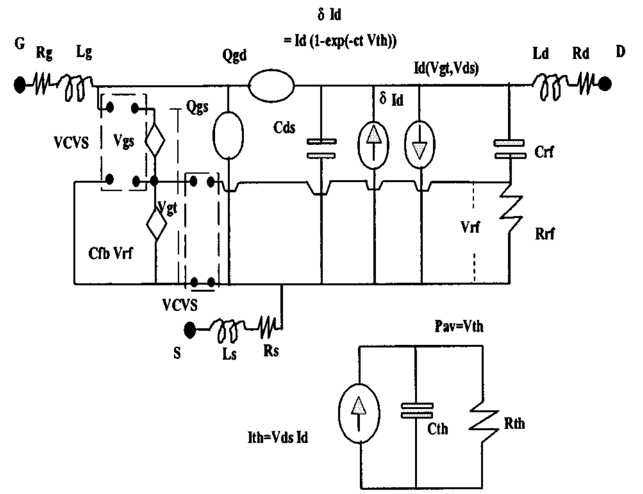

Fig. 1. Large-signal equivalent circuit of the transistor that including a RF feed-through loops and a sub-thermal circuit.

II. Model Formulation

A generalized equivalent circuit of a large-signal model of pseudomorphic high electron-mobility transistors (pHEMTs) has been reported elsewhere [4]. Fig. 1 shows the equivalent circuit of the device. The model for the enhancement mode (E-mode) device is essentially the same as that for the depletion-mode device. However, it requires more accurate fitting since the $I_{\rm dss}$ and capacitance behavior become more critical. The model has a thermal sub-circuit and a feedback circuit utilized for modeling of self-heating and accounting for the difference between RF-$G_{\rm ds}$ and dc-$G_{\rm ds}$.

The dc characteristics are defined as follows (refer to [4] for parameters c_t and $c_{\rm fb}$) [2]:

$$I_{\rm ds} = I_o \exp\left(-c_t P_{\rm av}\right) 0.5 \left(1 + \tanh\left(\frac{V_{\rm gs} - V_{\rm go}}{V_{\rm det}}\right)\right) \quad (1)$$

$$I_o = \frac{I_{\max}}{2}(1 + \tanh\phi)(1 + kV_{\rm ds}) \times \tanh\left(\left(a + \eta(0.95 - V_{\rm gs})\right) V_{\rm ds}\right) \quad (2)$$

and

$$\phi = P_1 x + P_2 x^2 + P_3 x^3 \quad (3)$$

$$x = V_{\rm gt} - V_{\rm to} + V_{\rm ds}\gamma \quad (4)$$

$$V_{\rm gt} = V_{\rm gs} + V_{\rm rf} C_{\rm fb}. \quad (5)$$

In expressions $I_{\max}$, P_1, P_2, P_3, and k, γ and η are fitting parameters. $P_{\rm av}$ is the average device power dissipation in operation with a thermal constant, $V_{\rm rf}$ is the node-voltage coupled from the drain port via an C–R circuit. $C_{\rm fl}$, accounts for the dispersion in $G_{\rm ds}$. Unlike conventional models, in which a $V_{\rm gs}$ independent RF conductance is assumed, $G_{\rm ds}$ along with the dispersion in our model vanishes below pinchoff. This eliminates the problem of a major PAE reduction at higher power drive caused by the limitation of dynamic load line by the RF $G_{\rm ds}$ that would otherwise exist in all the region. In (1), parameters $I_{\rm go}$ and $V_{\rm det}$ are used to tune the $I_{\rm dss}$. The AOM model for capacitance, modified from Parker model, is expressed as follows:

$$V_n = \kappa V_{e1} + (1-\kappa)\frac{\left(V_{e1}+V_p\right)+\sqrt{\left(V_{e1}-V_p\right)^2+\delta^2}}{2} \tag{6}$$

$$V_{e1} = \frac{\left(V_{\rm gs}+V_{\rm gd}\right)+\sqrt{\left(V_{\rm ds}^2+a^2\right)}}{2}+\varepsilon\sqrt{\left(V_{\rm ds}^2+\delta_\delta^2\right)} \tag{7}$$

$$V_{e2} = \frac{\left(V_{\rm gs}+V_{\rm gd}\right)-\sqrt{\left(V_{\rm ds}^2+a^2\right)}}{2}+\varepsilon\sqrt{\left(V_{\rm ds}^2+\delta_\delta^2\right)} \tag{8}$$

$$Q_{\rm gs} = \frac{C_{\rm gso}V_{\rm bi}}{1-m\left(1-\left(1-\frac{V_n}{V_{\rm bi}}\right)^{1-m}\right)f_1}+C_{\rm gdo}V_{e2}f_2 \tag{9}$$

$$Q_{\rm gd} = \frac{C_{\rm gso}V_{\rm bi}}{1-m\left(1-\left(\frac{1-V_n}{V_{\rm bi}}\right)^{1-m}\right)f_2}+C_{\rm gdo}V_{e2}f_1 \tag{10}$$

with $C_{\rm gso}$, $C_{\rm gdo}$, m, V_p, $V_{\rm bi}$, κ, δ, and δ_δ being the fitting parameters. f_1 and f_2 are the bilateral transition factor and are expressed as

$$f_{1,2} = 0.5\left(1\pm\tanh\left(\frac{3V_{\rm ds}}{\delta_\delta}\right)\right). \tag{11}$$

It was previously verified that these formulas satisfy charge conservation [4]. There are no conditional expressions in IV and QV equations and, therefore, they have continuous derivatives to any order. The continuity in derivatives is a prerequisite requirement for correct simulation of the third-order distortion and the linearity [3]. The parameter extraction started with deembedding the small-signal equivalent circuit at various biases. Gate forward conduction was taken into account in deembedding to avoid errors in gate–capacitance extraction. The extraction was performed using our in-house program ALPHAEXT. Figs. 2 and 3 show the modeled (line) and measured (symbol) $C_{\rm gs}$ and $C_{\rm gd}$, respectively, as function of $V_{\rm gs}$ with $V_{\rm ds}$ being a parameter. It is seen that the model predicts very well the pinchoff in capacitance $C_{\rm gs}$ and $C_{\rm gs}$ versus $V_{\rm gs}$. The pinchoff behavior is essential since most of the period of the gate voltage swing is well below the pinchoff at a higher power. An improper capacitance model may result in great discrepancy.

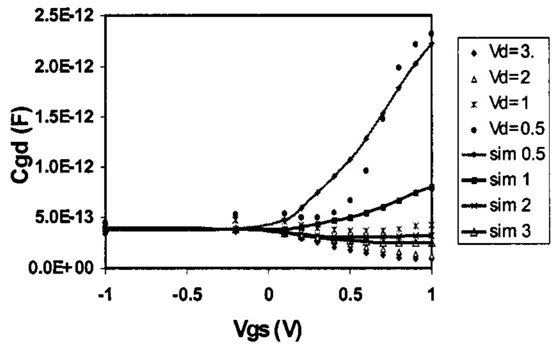

Fig. 2. Measured and fitted gate–drain capacitance versus gate voltage for $V_{\rm ds} = 0.5, 1, 2$, and 3, respectively.

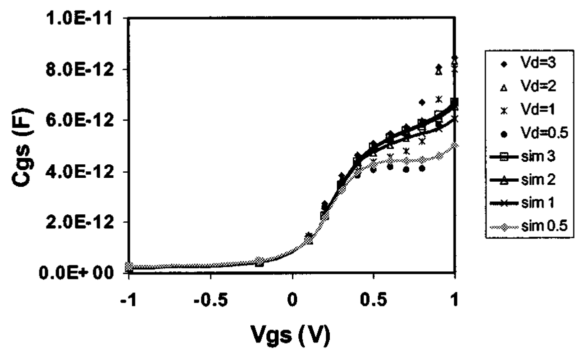

Fig. 3. Measured and fitted gate–source capacitance versus gate voltage for $V_{\rm ds} = 0.5, 1, 2$, and 3, respectively, and total gatewidth of 2 mm.

III. Model Verification

The E-pHEMT under study has a gate length of 0.7 μm and a total gatewidth of 2 mm. The model extraction is based on dc characteristics and bias-dependent S-parameters. The frequency range is from 0.2 to 15.2 GHz and the bias range for $V_{\rm ds}$ is from 0.25 to 5 V and $V_{\rm gs}$ is from -3 to 1 V. The wide bias range is needed to ensure broad-ranged fitting in *IV* and *CV* characteristics. The bias-dependent element values are then fitted to the model formulas to obtain the model parameters.

Other sized devices up to 32 mm of total gate periphery were also characterized. A special scaling rule is developed for the distributed effects [6]. The model is then coded into Libra SeriesIV by compiling a senior element.

Fig. 4 compares the measured and modeled dc characteristics. It is seen that the fitting is fairly good. Fig. 5 plots the measured and modeled S-parameters at $V_{\rm ds} = 3$ V and $V_{\rm gs} = 0.3$ V. The scaling rule was also checked by comparing the simulated S-parameters to the measured data for various size of devices at a same bias condition. Good agreement is found for all those comparisons.

Fig. 6 shows the modeled and measured power performance for a 4-mm E-pHEMT under 50-Ω source and 50-Ω load conditions. The agreement in output power, power gain, and PAE indicates the validity of the scaling rule.

IV. Load–Pull Simulation

To achieve the best power performance, it is essential to find the optimum loads at the fundamental and at harmonics as well. A two-port harmonic load element is created in SeriesIV as a

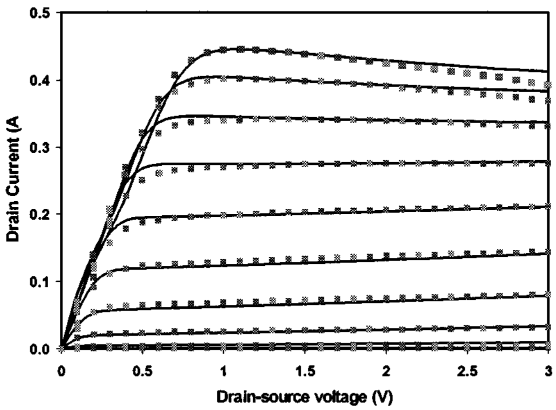

Fig. 4. Modeled (line) and measured (symbol) dc characteristics.

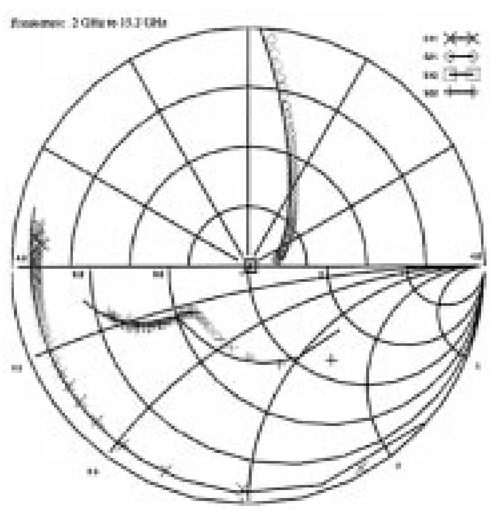

Fig. 5. Modeled (line) and measured (symbol) S-parameters. $V_{\rm ds} = 3$ V, $V_{\rm gs} = 0.3$ V.

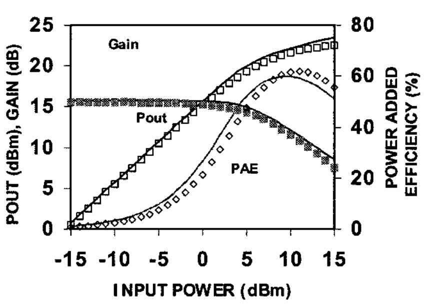

Fig. 6. Modeled (line) and measured (symbol) output power gain and PAE for a 4-mm device. $V_{\rm ds} = 3$ V, $I_{\rm do} = 50$ mA.

senior element in that the magnitude and phase of S-parameters are specified at each harmonic. In order for it to be lossless, the S-parameter matrix is written to be unitary.

Load–pull simulation is performed at $f = 0.9$ GHz and $P_{\rm in} = 9$ dBm for a 2-mm E-pHEMT. A load–pull system from ATN Microwave Inc., Billerica, MA, was employed in the measurement. Fig. 7 plots the PAE versus the second harmonic load impedance. The source and load at the fundamental are set to be a tradeoff between the best PAE and maximum output

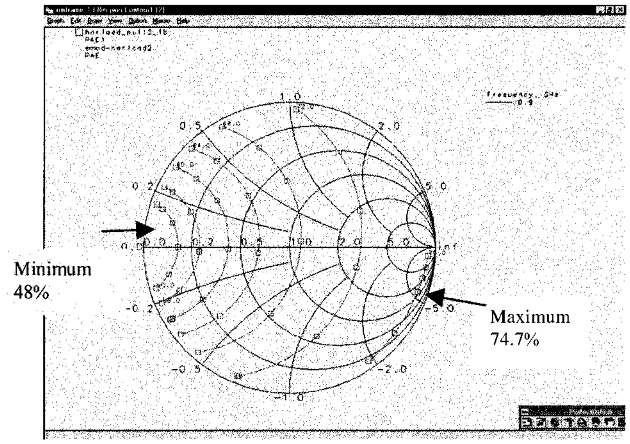

Fig. 7. PAE (%) versus second harmonic load at $f = 0.9$ GHz and $P_{\rm in} = 9$ dBm for 2-mm device. $V_{\rm ds} = 3.2$ V, $I_{\rm do} = 50$ mA.

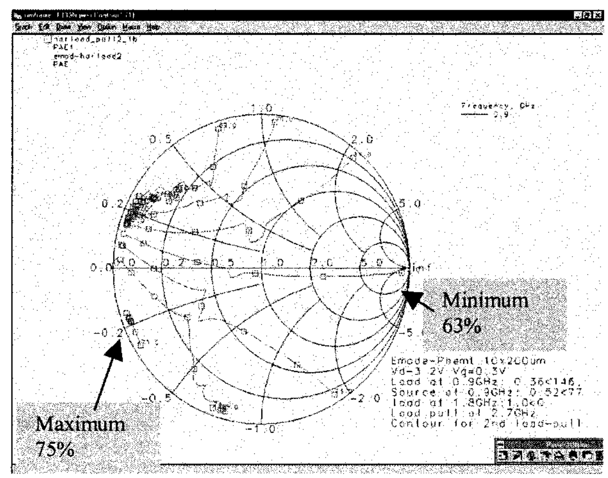

Fig. 8. PAE (%) versus third harmonic load at $f = 0.9$ GHz and $P_{\rm in} = 9$ dBm for 2-mm device. $V_{\rm ds} = 3.2$ V, $I_{\rm do} = 50$ mA.

power, namely, $0.52\angle 76.8^\circ$ for the source and $0.36\angle 148^\circ$ for the load.

It is seen that the optimum load at second harmonic is an open circuit with maximum $\mathrm{PAE} = 74.7\%$, whereas the worst case is a short-circuited load with $\mathrm{PAE} = 48\%$. Next, after fixing the second harmonic load to be an open, we simulate the load–pull at the third harmonic, and the results are plotted in Fig. 8. It is found that the optimum reflection for it is about $1\angle 210^\circ$, where the $\mathrm{PAE} = 75\%$ and the worst point is about $1\angle 90^\circ$, where $\mathrm{PAE} = 63\%$. Fig. 9 shows the measured results for second harmonic load–pull. The solid-state tuner has a limited tuning range for second harmonic covering about ~0.8 of the Smith chart. In spite of the limited tuning range, it is clearly seen that the optimum second load is indeed close to the open side, namely, at $0.77\angle 0^\circ$, with $\mathrm{PAE} = 72.4\%$, while the worst loading is only slightly deviated from a short circuit with somewhat inductive. Its phase is about $7\pi/8$. Fig. 10 shows the measured power performance with the second harmonic termination set at $0.75\angle -10^\circ$. Also shown is the comparison with simulated results at two harmonic loading conditions, the second: both use $0.75\angle -10^\circ$, and the third: open or short. The measured PAE

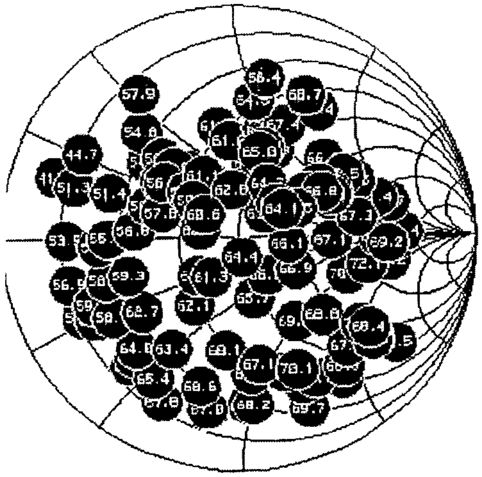

Fig. 9. Measured PAE (%) load–pull results at second harmonic at $f = 0.9$ GHz and $P_{\rm in} = 9$ dBm. $V_{\rm ds} = 3.2$ V and $I_{\rm do} = 50$ mA for a 2-mm device. The maximum is at the right end and the minimum is at the left end. PAE: $>72\%$ verses $<50\%$.

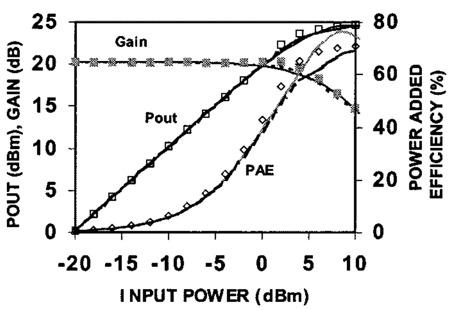

Fig. 10. Modeled (line) and measured (symbol) output power; power gain and PAE for the 2-mm device. $V_{\rm ds} = 3.2$ V, $I_{\rm do} = 50$ mA. $f = 0.9$ GHz. Solid line: second load: $0.75\angle-10^{\circ}$, third load: short broken line: second load: $0.75\angle-10^{\circ}$, third load: open symbol: second load: $0.75\angle-10^{\circ}$, third load: unknown.

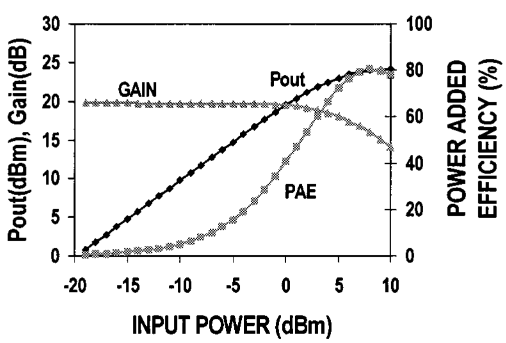

Fig. 11. Simulated power performance of 2-mm E-mode pHEMT under optimum loading and harmonic tuning conditions.

results at high power region are just in between these two extremes. Considering that the third harmonic is unknown in the measurement, the agreement is really good and, thus, the model is verified.

By optimizing the fundamental loading, as well as the second and third harmonics loading, the PAE as high as 80% can be achieved. The optimum loading for maximum PAE at fundamental is $0.23\angle148^{\circ}$ and for the source termination is $0.52\angle77^{\circ}$. The optimum loading at the second harmonic remains to be an open circuit, whereas the third harmonic termination is close to a short circuit. Fig. 11 shows the simulated power performance. It is seen that the PAE is as high as 80%. The PAE as high as 80% has been achieved with more devices in more extended load–pull measurements.

The harmonic tuning for best PAE is opposite to the conventional class F, where the second harmonic is set at short and the third harmonic is set at open. We have found that our new mode has higher efficiency than class F at a bias class-AB condition. Although the device in this paper is an E-mode pHEMT, this high-efficiency mode can be equally applied to other power transistors, such as a D-mode FET and heterojunction bipolar transistor (HBT).

V. Conclusions

A comprehensive and accurate model has been developed for an E-mode pHEMT. The model takes into account charge conservation, capacitances near and below pinchoff, and dispersions. Additional parameters are used to fit the $I_{\rm dss}$. In conjunction with a harmonic load element in simulation, the model successfully predicts the power performance and optimum harmonic loading. As high as 80% PAE can be achieved under optimum loading and with harmonic tuning. It is found that the optimum PAE can be obtained by tuning the second harmonic at a vicinity of open and third harmonic at close to short. The model is verified by comparing the simulated dc RF characteristics and power performance to the measured results.

References

[1] Y. Tkachenko, A. Klimashov, C. Wei, and D. Bartle, "Enhancement mode PHEMT for single supply high efficiency power amplifiers," presented at the Eur. Microwave Workshop, Munich, Germany, 1999.

[2] I. Angelov, "Chalmers nonlinear HEMT and MESFET model," Chalmers Univ. Technol., Göteborg, Sweden, Rep. 26, 1996.

[3] A. E. Parker and D. J. Slellern, "A realistic large-signal MESFET model for SPICE," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1563–1570, Sept. 1997.

[4] C. J. Wei, Y. A. Tkachenko, and D. Bartle, "An accurate large-signal model of GaAs MESFET which accounts for charge conservation, dispersion, and self-heating," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1638–1644, Nov. 1998.

[5] J. Staudinger, "Multiharmonic load termination effects on GaAs MESFET power amplifiers," *Microwave J.*, vol. 39, pp. 60–77, Mar. 1996.

[6] C. J. Wei, Y. A. Tkachenko, and D. Bartle, "Scalable small-signal MESFET/PHEMT models up to 30 mm periphery," in *Asia–Pacific Microwave Conf. Dig.*, Singapore, 1999, pp. 52–55.

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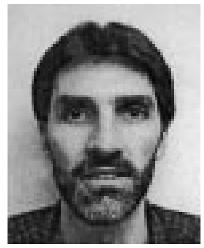

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